

CLAIMS

We claim:

1 1. A structure for testing external connections to
2 semiconductor devices, the structure comprising:
3 an external electrical path between selected external
4 connections on the semiconductor devices.

1 2. The structure according to claim 1, wherein the
2 external electrical path comprises a thin film interface
3 probe.

1 3. The structure according to claim 1, wherein the
2 external electrical path ^{interfaces} [permits] a driver from an
3 input/output to [interface to] a receiver of a corresponding
4 paired input/output.

1 4. The structure according to claim 1, wherein the
2 external connections on the semiconductor devices are C4
3 connections.

1 5. The structure according to claim 1, wherein the

2 structure carries out boundary scan and input/output wrap
3 test techniques.

1 6. The structure according to claim 1, wherein all
2 adjacent input/output pairs are paired.

1 7. The structure according to claim 1, wherein the
2 structure provides a high frequency closed loop self test of
3 drivers and receivers.

1 8. The structure according to claim 1, wherein the
2 structure is extendible to full wafer contacting for burn-in
3 and test.

1 9. The structure according to claim 1, wherein the
2 external electrical path comprises:

3 a thin film of electrically insulating material;
4 a plurality of passages through the thin film of
5 electrically insulating material, wherein the passages are
6 arranged in a pattern corresponding to a pattern of external
7 connections on the semiconductor device;
8 electrically conducting material arranged in the
9 plurality of passages; and

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10 electrical connections between the electrically
11 conducting material in selected pairs of the plurality of
12 passages.

1 10. The structure according to claim 9, further
2 comprising:
3 a space transformer connected to the electrically
4 conducting material arranged in the plurality of passages.

1 11. The structure according to claim 1, wherein the
2 external electrical path is provided between pairs of
3 external connections on the semiconductor devices.

1 12. The structure according to claim 1, wherein the
2 external electrical path is provided between a plurality of
3 external connections on the semiconductor devices.

1 13. The structure according to claim 1, wherein the
2 external electrical path is provided between non-adjacent
3 external connections on the semiconductor devices.

1 14. A method for testing external connections to a
2 semiconductor device, the method comprising:

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3 providing an external electrical path between selected
4 external connections on the semiconductor devices; and
5 carrying out the testing by sending at least one signal
6 through the external electrical path.

1 15. The method according to claim 14, wherein the test
2 comprises at least one of a boundary scan and input/output
3 wrap test.

1 16. The method according to claim 14, further
2 comprising:
3 pairing all adjacent input/output pairs.

1 17. The method according to claim 14, wherein the test
2 comprises a high frequency closed loop self test of drivers
3 and receivers.

1 18. The method according to claim 14, wherein the test
2 comprises burn-in.

1 19. The method according to claim 14, further
2 comprising:
3 interfacing a driver from an input/output to a receiver

4 of a corresponding paired input/output.

1 20. The method according to claim 14, wherein
2 providing the external electrical path comprises:

3 providing a thin film of electrically insulating
4 material;

5 providing a plurality of passages through the thin film
6 of electrically insulating material, wherein the passages
7 are arranged in a pattern corresponding to a pattern of
8 external connections on the semiconductor device;

9 providing electrically conducting material arranged in
10 the plurality of passages; and

11 providing electrical connections between the
12 electrically conducting material in selected pairs of the
13 plurality of passages.

1 21. The method according to claim 20, further
2 comprising:

3 providing a space transformer connected to the
4 electrically conducting material arranged in the plurality
5 of passages.

1 22. The method according to claim 14, wherein the

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2 external electrical path is provided between pairs of
3 external connections on the semiconductor devices.

1 23. The method according to claim 14, wherein the
2 external electrical path is provided between a plurality of
3 external connections on the semiconductor devices.

1 24. The method according to claim 14, wherein the
2 external electrical path is provided between non-adjacent
3 external connections on the semiconductor devices.

1 25. A method for forming a structure for testing
2 external connections to semiconductor devices, the method
3 comprising:

4 providing a thin film of electrically insulating
5 material;

6 providing a plurality of passages through the thin film
7 of electrically insulating material, wherein the passages
8 are arranged in a pattern corresponding to a pattern of
9 external connections on the semiconductor device;

10 providing electrically conducting material in the
11 plurality of passages; and

12 providing electrical connections between the

13 electrically conducting material in selected passages.

1 26. The method according to claim 25, wherein
2 providing the electrical connections between the
3 electrically conducting material in the selected passages
4 comprises providing electrically conducting material on the
5 thin film of electrically insulating material between the
6 selected passages.

1 27. The method according to claim 25, wherein the
2 selected passages are adjacent pairs.

1 28. The method according to claim 25, wherein the
2 electrical connections are provided between a plurality of
3 passages.

1 29. The method according to claim 25, wherein the
2 electrical connections are provided between non-adjacent
3 passages.